

# A SPICE MODEL FOR IGBTs

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*SPICE is the most popular program for simulating the behavior of electronic circuits. The biggest stumbling block that engineers run into is turning vendor data sheet specifications into SPICE models that emulate real devices and run without convergence problems. This is especially true for power devices, like IGBTs, where the cost of testing and possibly destroying devices is prohibitive. The following paper describes the FIRST known SPICE subcircuit macro model for IGBTs[1].*

## Introduction

You've finally tested a version of your design that seems to work well, but you would feel a lot better if you KNEW the circuit would work well with all the devices that the vendor will supply in production. You found a model in a library, but you are not sure what specifications from the data book apply to that model. The following paragraphs will try to clarify the relationship between data book specifications and a new Insulated Gate Bipolar Transistor (IGBT) subcircuit SPICE model.

## Modeling An IGBT

An IGBT is really just a power MOSFET with an added junction in series with the drain. This creates a parasitic transistor driven by the MOSFET and permits increased current flow in the same die area. The sacrifice is an additional diode drop due to the extra junction and turn-off delays while carriers are swept out of this junction.

Figure 1 shows a simplified schematic of an IGBT. Note that what is called the "collector" is really the emitter of the parasitic PNP. What we have is a MOSFET driving an emitter follower. Although this model is capable of producing the basic function of an IGBT, refinements are required for more accurate modeling and to emulate the non-linear capacitance and breakdown effects.

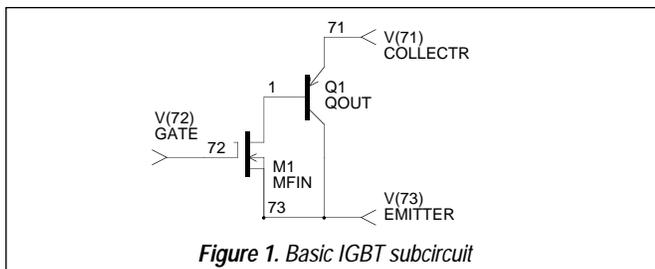


Figure 1. Basic IGBT subcircuit

## Expanded IGBT Model

Figure 2 shows the complete subcircuit. Table 1 shows the corresponding SPICE 2G.6 compatible subcircuit netlist for an International Rectifier IRGBC40U device [2]. The subcircuit is generic in nature, meaning, that component values in the subcircuit can be easily recalculated to emulate different IGBT devices. The model accurately simulates, switching losses, nonlinear capacitance effects, on-voltage, forward/reverse breakdown, turn-on/turn-off delay, rise time and fall tail, active output impedance, collector curves including mobility modulation.

Let's discuss the subcircuit one component at a time:

Q1 is a PNP transistor which functions as an emitter-follower to increase the current handling ability of the IGBT. BF (Forward Beta) is determined by the step in the turn-off tail which indicates the portion of the current handled by the PNP. TF (Forward Transit Time) controls

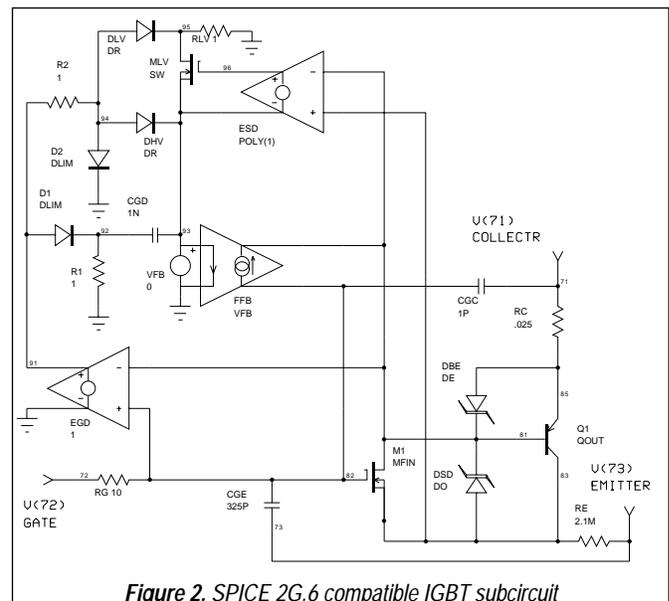


Figure 2. SPICE 2G.6 compatible IGBT subcircuit

Table 1. IRGBC40U IGBT Subcircuit

```
.SUBCKT IRGBC40U 71 72 74
*
*   TERMINALS:  C  G  E
*   600 Volt 40 Amp 6.04NS N-Channel IGBT 06-13-1992
Q1 83 81 85 QOUT
M1 81 82 83 83 MFIN L=1U W=1U
DSD 83 81 DO
DBE 85 81 DE
RC 85 71 21.1M
RE 83 73 2.11M
RG 72 82 25.6
CGE 82 83 1.42N
CGC 82 71 1P
EGD 91 0 82 81 1
VFB 93 0 0
FFB 82 81 VFB 1
CGD 92 93 1.41N
R1 92 0 1
D1 91 92 DLIM
DHV 94 93 DR
R2 91 94 1
D2 94 0 DLIM
DLV 94 95 DR 13
RLV 95 0 1
ESD 96 93 POLY(1) 83 81 19 1
MLV 95 96 93 93 SW
LE 73 74 7.5N
.MODEL SW NMOS (LEVEL=3 VTO=0 KP=5)
.MODEL QOUT PNP (IS=377F NF=1.2 BF=5.1 CJE=3.48N
+ TF=24.3N XTB=1.3)
.MODEL MFIN NMOS (LEVEL=3 VMAX=400K THETA=36.1M ETA=2M
+ VTO=5.2 KP=2.12)
.MODEL DR D (IS=37.7F CJO=100P VJ=1 M=.82)
.MODEL DO D (IS=37.7F BV=600 CJO=2.07N VJ=1 M=.7)
.MODEL DE D (IS=37.7F BV=14.3 N=2)
.MODEL DLIM D (IS=100N)
.ENDS
```

the turn-off tail time. The OFF control parameter can be added to aid DC convergence by starting DC calculations with Q1 turned off.

MOSFET M1 emulates the input MOSFET [3, 4]. The Berkeley SPICE Level=3 model is used in the .MODEL MFIN statement in order to better model modern device characteristics. VMAX (Maximum Drift Velocity) controls the collector (drain) curves in the saturation region, and hence the VCE(on) voltage. THETA (Mobility Modulation Parameter) is used to reduce the gain at high gate voltages which is normally exponential. ETA (Static Feedback) is similar to the “Early effect” in bipolar transistors and is used to control the slope of the collector curves in the active region and hence the output impedance. VTO (Threshold Voltage) is directly proportional to Gate Threshold Voltage VGE(th). KP (Intrinsic Transconductance) is related to the test parameter gfe (Forward Transconductance) but must be adjusted for VTO, VMAX, THETA, and ETA.

DSD emulates the source-drain (substrate) diode, its capacitance, and forward breakdown voltage. VJ and M have been adjusted to better emulate the (Coes) capaci-

tance curve. This diode includes breakdown voltage and capacitor CBD as CJO. DBE, the B-E diode of the output transistor, emulates the reverse breakdown of the PNP base-emitter junction (and of the IGBT). IS is made small and N large to avoid shunting the junction in the forward direction.

RC, the collector resistance, represents the resistive part of VCE(on). With the B-E diode, RC controls the VCE(on) voltage. RE, the emitter ohmic resistance, provides the feedback between emitter current and gate voltage. RG, the gate resistance, combines with the gate capacities in the subcircuit to help emulate the turn-on and turn-off delays, and the rise and fall times.

CGE, the Gate-to-Emitter capacitor, equals Cies minus Cres. CGC, the Gate-to-Collector capacitor, is a fixed capacitor representing package capacitances which are important at high voltages where Cres is small.

There are nine parts that replace the CGDO capacitor to more accurately model the change in capacitance with gate and drain voltage [5]. EGD is a voltage generator equal to M1’s gate-to-drain voltage which is used to supply voltage to the feedback capacitance emulating subcircuit. VFB is a voltage generator used to monitor the current in the feedback capacitance emulation subcircuit for FFB. FFB is a current controlled current source used to inject the feedback current back into M1. EGD, VFB, and FFB provide the necessary power to drive the feedback components in parallel without loading M1. They also permit ground connections in the subcircuit, improving convergence and accuracy. CGD is the fixed part of the gate-to-drain capacitor. R1 and D1 limit its operation to the region where the gate voltage exceeds the drain voltage. DHV is a diode which emulates the gate-to-drain capacitor at high voltages. R2 and D2 limit its operation to the region where the drain voltage exceeds the gate voltage. DLV is a diode which emulates the gate-to-drain capacitance variation with drain voltages (variable part of Cres) below the transition voltage. The multiplier ( $=C1/C2 - 1$ ) used is determined by the size of the capacitance step needed. RLV shunts its current to ground at higher voltages. ESD is a voltage controlled voltage source that senses source-to-drain voltage and drives MLV. The POLY form is used so that the proper offset voltage can be inserted without an additional element. MLV is used as a switch to disconnect DLV from the feedback at higher voltages, emulating the drastic reduction in feedback capacitance with voltage found in most modern IGBTs.

SpiceMod		
SPICEMOD 2.1 ===== IGBT (X) ===== 12-14-1994		
.SUBCKT Name <IRGBC40U>	= IRGBC40U	Affects:
Channel Type <N,P>	= N	BU in DO
Collector-to-Emitter Breakdown Volt, BU CES	= 600.000 U.	BU in DE
Emitter-to-Collector Breakdown Volt, BU ECS	= 15.000 U.	All Parameters
Max. Continuous Collector Current, ICmax	= 40.000 A.	RC, RS
C-to-E Saturation Voltage, UCE(on)	= 2.700 U.	
at <Maximum> Test Current, IC(on)	= 40.000 A.	
and <Maximum> Bias, UCE(on)	= 15.000 U.	
Gate Threshold Voltage, UGE(th)	= 5.200 U.	UTO
Forward Transconductance, gfe	= 14.000 S.	KP
at <ICmax/2> Current, IC	= 20.000 A.	
Output Conductance, goe	= 80.267 mmohs	LAMBDA, ETA
Capacitance Test Voltage, UCE	= 30.000 U.	<above UCT>
Input Capacitance, Cies	= 1429.630 pF.	CGE
Output capacitance, Coes	= 194.430 pF.	CBD <CJO in DO>
Reverse Transfer Capacitance, Cres	= 7.027 pF.	CGD <CJO in DR>
Capacitance Transition Voltage, UCT	= 19.000 U.	ELU offset
Capacitance Shift in Cres at UCT, <C1/C2>	= 14.000	DLU multiplier
Resistance for Switching Tests, Rgen	= 10.000 Ohms	RG
Turn-Off Delay Time, td(off)	= 145.465 ns.	RG
Fall Time, tf	= 97.461 ns.	TF
Current Step at Turn-Off, <I2/I1>	= 0.836	BF
Emitter Lead Inductance, Le	= 7.500 nH.	LE (<0 = none>)
SELECT WITH ARROWS, TYPE DATA F1=HELP F2=SUBCKT F3=RESET DATA Exc=EXIT/SAVE		

Figure 3, Data sheet parameters (above left) used to create the SPICE IGBT subcircuit (Table 1). To make a new model, data sheet values are entered into the SpiceMod entry screen. As they are entered the subcircuit values are calculated. The more data that is entered, the more accurate the final model will be. The subcircuit parameters affected by each entered parameter are shown to right.

LE emulates the emitter lead inductance. 7.5 nano-henries represents the lead inductance of a TO-220 plastic package. The total lead inductance Le is an important high speed limit parameter and should include all external lead inductance through which output current flows before it reaches the common ground with the drive circuit. The inductance of the drain and gate leads have little effect on simulations but could be easily added to the subcircuit. You may, however, want to add in 7 nH per cm. or 18 nH per inch for any PCB traces or wires. Typical internal inductances are: TO-220 (plastic): 7.5 nH, TO-218 (plastic): 8 nH (1 bond wire), 4 nH (2 wires), TO-204 (TO-3) (metal): 12.5 nH [6].

### Software Solution To Modeling Headaches

If entering and adjusting all of these parameters seems a little too complex and time-consuming, you can take the easy way out and generate your IGBT subcircuit using SPICEMOD, a general purpose SPICE modeling program that supports IGBT model development. SPICEMOD derives SPICE parameters from generally available data book information. The most unique feature of SPICEMOD is its estimation capability. If some of the data sheet parameters are not available, SPICEMOD will provide estimates for data not entered based on the data that is entered. Thus, SPICEMOD will never leave a key SPICE parameter at its default value. This is the downfall of many modeling programs and can cause the resulting SPICE model to be invalid. Figure 3 shows the input parameters from the data book and the SPICE parameters that are primarily affected

by each input for the device in Table 1.

SPICEMOD is so intelligent that a reasonable first order device model can be obtained by simply entering the voltage and current ratings of the device. Of course, the more data entered, the more accurate the final model. In addition to IGBTs, SPICEMOD also produces models for diodes, zeners, BJTs, JFETs and MOSFETs, and subcircuit macromodels for power transistors, Darlington transistors, power MOSFETs, and SCRs [7]. All of the models are

Berkeley SPICE 2G compatible and can be used with any SPICE program on any computer platform. Detailed next are the DC and Transient performance characteristics of the outlined IGBT model.

### IGBT Testing

Figure 4 shows the output characteristics of the IRGBC40U as simulated by IsSpice4, a native mixed mode SPICE 3F based simulator. Note the offset from zero caused by the base-emitter diode of the PNP. The slight slope of the curves, controlled by ETA, represents the output impedance. The values are well within the data sheet tolerances without any need for optimization. This is not surprising given the possible variation in the device's gfe. However, it is easy to see that with the simple circuits provided here, it is quite easy to tweak the model performance for a given situation.

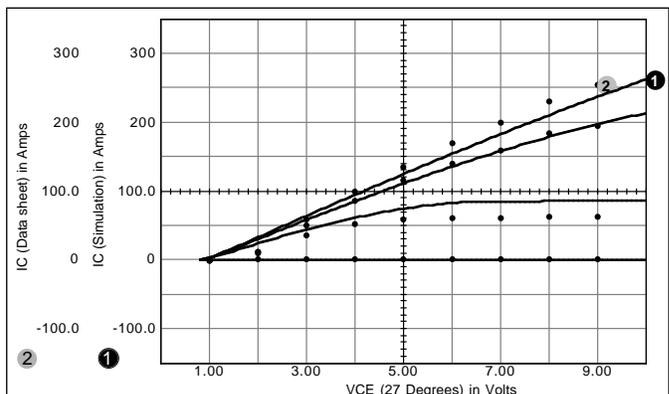


Figure 4. Data sheet (waveform 2, dots) and simulated (waveform 1, solid) output characteristics for the IRGBC40U.

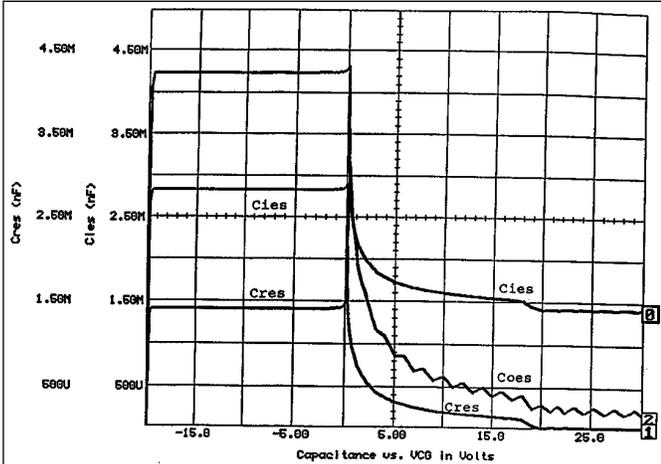


Figure 5. Simulated capacitance characteristics for the IRGBC40U. All waveforms are scaled the same.

The model exhibits forward and reverse breakdown effects. Although not normally operated in these modes, inductive flyback effects can easily drive an IGBT into one or both of these regions. Because IGBTs are frequently used in switching power supplies, this is not an unusual occurrence. Excess energy in reverse breakdown was a frequent killer of early IGBTs.

Figure 5 shows the capacitance variations versus gate and collector voltages for the model. The X-axis is collector-to-gate voltage, so the left part with negative voltages actually represents positive gate voltage while the right part represents positive collector voltages.

Note that all capacitance tests are made with the IGBT in a non-conducting mode. In normal operation the capaci-

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TSWITCH.CIR - Device Switching Characteristics
.PRINT TRAN V(3) V(4,3) V(5,6) V(6) I(VC)
.IC V(6)=0
.TRAN 2N 1000N
*ALIAS V(6)=ESW
*ALIAS V(3)=VOUT
RIN 1 2 10 ;SET TEST R(GEN)
X1 30 2 0 IRGBC40U ;REPLACE WITH YOUR DEVICE NAME
VC 3 30
IL 0 4 20 ;SET TEST CURRENT
RL 3 4 .01
GPWR 0 5 POLY(2) 3 0 4 3 0 0 0 100
* MULTIPLIES VOLTAGE AND CURRENT TO YIELD POWER AS V(5,6)
RPWR 5 6 1
CEN 6 0 1 ;INTEGRATES POWER TO GIVE ENERGY/PULSE AS V(6)
D2 0 4 DZEN
.MODEL DZEN D(BV=480 IBV=.001)
* ^ SET TEST VOLTAGE
REN 6 0 1E6 ;PROVIDES DC PATH TO GROUND
VIN 1 0 PULSE 0 15 0 1N 1N 200N 1000N
.END

```

Figure 6. The switching circuit TSWITCH.CIR (below) used to test the transient IGBT performance.

tive feedback current is multiplied by  $(BF+1)$  at the output, so BF is an important parameter.

The circuit in Figure 7 (TSWITCH.CIR) is used to simulate various switching effects. The current generator available in IsSpice4 replaces the inductor and two other switching devices normally used for this test. Note the two-input voltage controlled current source that is added to multiply the IGBT voltage and current to compute power (measured across the one-ohm resistor). This power (current) is then integrated by the capacitor CE to get energy (as voltage). The multiplication and integration could have just as easily been done in a SPICE post-processing program. However, when the waveforms are calculated by IsSpice4 the simulated waveforms can be cross-probed directly on the schematic as shown in Figure

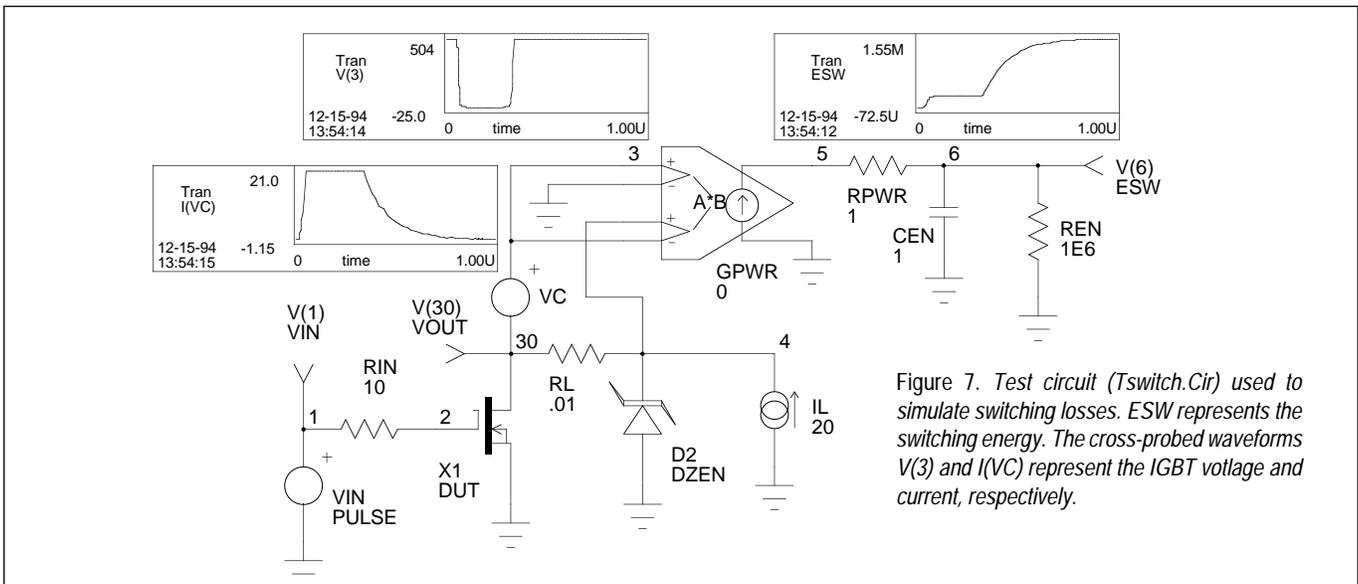


Figure 7. Test circuit (Tswitch.Cir) used to simulate switching losses. ESW represents the switching energy. The cross-probed waveforms V(3) and I(VC) represent the IGBT voltage and current, respectively.

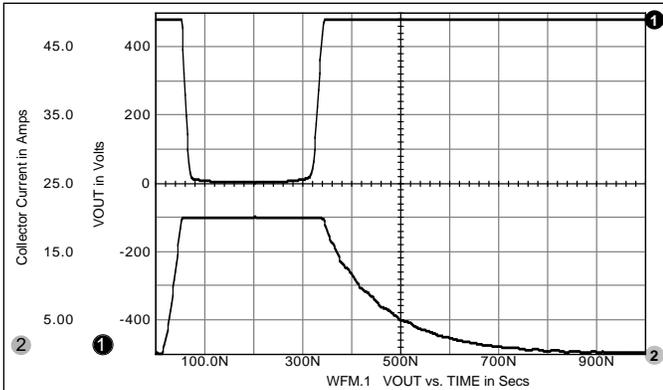


Figure 8. Switching losses are calculated by multiplying the current and voltage waveforms during the switching period.

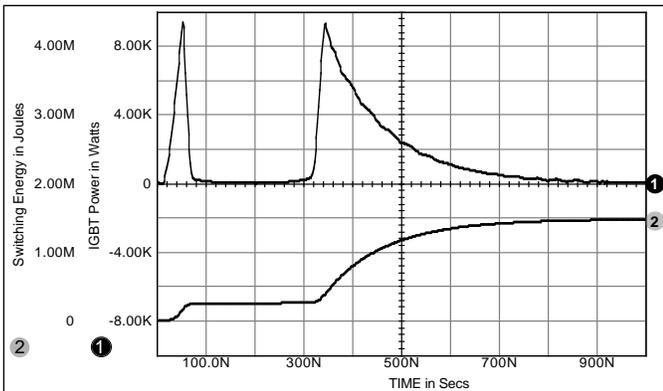


Figure 9. The instantaneous power (waveform 1) and cumulative energy (waveform 2) curves which match the curves in figure 8.

7. It should be noted that the data sheet values for switching characteristics can be greatly affected by the test circuit and test load used. Care should be given to properly constructing the test circuit based on the data sheet information, otherwise the simulation results may not be comparable with the actual performance.

Switching losses are calculated by multiplying the IGBT current and voltage waveforms during the switching period (figure 8). Note that the voltage does not begin to fall until the current reaches maximum and that the current does not begin to fall until the voltage reaches maximum. Note the long tail on the current waveform due to the PNP (controlled by TF).

Figure 9 shows the instantaneous power and cumulative energy curves which match the curves in Figure 8. Note that the scale is millijoules, so the final value is 1.5 millijoules.

## Temperature Effects

Diode voltage shifts due to temperature are properly modeled by SPICE, but others are not well emulated. Resistive shifts with temperature can be approximated by adding a temperature coefficient to RC (`RC 85 71 21.1M TC=.01` for SPICE 2, or `RC 85 71 21.1M RMOD & .MODEL RMOD R TC1=.01` for SPICE 3). This was not included in the subcircuit because it can cause error messages due to differences in SPICE implementations from some vendors. Temperature effects can best be handled by entering data book parameters at temperature into the subcircuit for an accurate high temperature model.

## Example Usage: 3 Phase IGBT Inverter

As a practical example, a 3 phase inverter with simplified motor load was simulated (Figure 10). The IGBT model allows examination of both circuit and IGBT related design issues. For the inverter circuit, Figure 10 shows the line-line and line-neutral quantities, as well as the IGBT switching waveforms. In Figure 11, the effect of varying the load inductances (LA, LB, and LC) is displayed. The control circuitry has been simplified so as not to unnecessarily complicate the simulation. An anti-parallel diode has been included in the IGBT subcircuit used in this simulation by adding a diode from nodes 74 to 71. For those of you who think that such simulation are beyond the capability of PC, on a 90MHz Pentium the 166 element inverter circuit runs in 28.05 seconds. On a 275MHz Digital Alpha AXP PC) it runs in under **6 seconds!!**

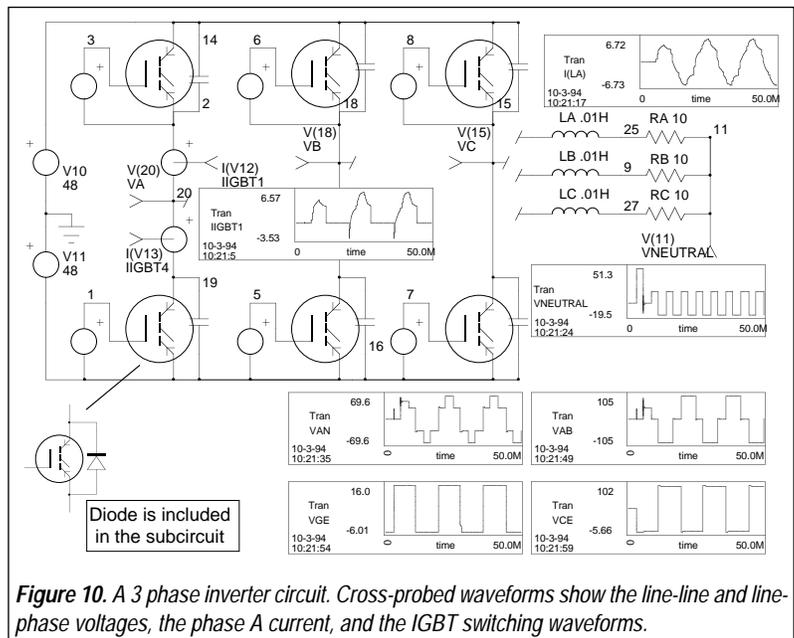
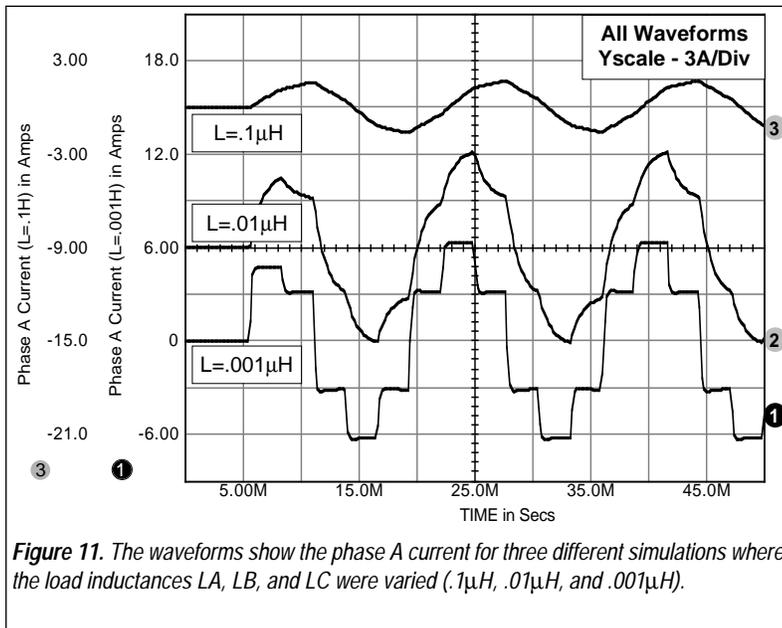


Figure 10. A 3 phase inverter circuit. Cross-probed waveforms show the line-line and line-phase voltages, the phase A current, and the IGBT switching waveforms.



Issues such as parallel IGBT operation, overcurrent/short circuit protection circuitry, and various snubber configurations can also be explored with the model.

### Conclusions and Future Work

There are a number of ways to better model the nonlinear gate-drain capacitance. An enhanced method using the SPICE 3 B element is described in [8]. It uses half the number of elements and allows alternate capacitance responses, such as a sigmoidal response, to be constructed. More importantly, [9] describes a new AHDL (Analog Hardware Description Language) based on 'C' that will allow much more accurate and efficient IGBT models to be developed.

A SPICE IGBT subcircuit has been developed that relates well to data book information. It models the DC collector family and on- voltages, non-linear capacitance effects, and switching characteristics. Forward and reverse breakdown characteristics are also included.

The model finally gives power engineers the ability to simulate all types of IGBT based circuits [9]. An intelligent modeling program has been introduced that quickly generates custom SPICE subcircuits from data supplied by the user and estimates reasonable values for any missing data by scaling from the supplied data.

### References

- [1] Charles E. Hymowitz, Intusoft Newsletter, "Intusoft Modeling Corner", Intusoft, June 1992, San Pedro, CA 90731
- [2] "Insulated Gate Bipolar Transistor Designer's Manual", International Rectifier, El Segundo, CA 90245
- [3] Andrei Vladimirescu and Sally Liu, "The Simulation of MOS Integrated Circuits Using SPICE", UCB/ERL M80/7, University of California, Berkeley, CA 94720
- [4] Paolo Antognetti and Giuseppe Massobrio, "Semiconductor Device Modelling with SPICE", McGraw-Hill, 1988
- [5] Charles-Edouard Cordonnier, Application Note AN-1043, "Spice Model for TMOS Power MOSFETs", Motorola Inc. 1989
- [6] Lawrence G. Meares and Charles E. Hymowitz, "Simulating with SPICE", Intusoft, San Pedro, CA 90731
- [7] SpiceMod User's Guide, Intusoft, June 1990, San Pedro, CA 90731
- [8] Charles E. Hymowitz, Intusoft Newsletter, "New Technique Improves Power Models", Intusoft, June 1992, San Pedro, CA 90731
- [9] Charles E. Hymowitz, Intusoft Newsletter, "3 Phase IGBT Inverter" & "New AHDL Based On 'C'", October 1994, San Pedro, CA 90731

Sample models for several IGBT devices are available free of charge on the Compuserve CADD/CAM/CAE Vendor forum, Library 21 (GoCADDVEN at any ! prompt) for Compuserve users and an ftp site (ftp.iee.ufrgs.br.) for Internet users. The SPICEMOD program is available from Intusoft, 222 W. Sixth Street, Suite 1070, San Pedro, CA 90731 Tel. (310) 833-0710, FAX (310) 833-9658